

WHAT IS CLAIMED IS:

1. A system for providing linearized operation of a RF circuit, said system comprising:
- a first transistor differential pair;
 - a second transistor differential pair;
 - a control signal input port;
 - a first control signal output port, wherein said first control signal output port is coupled to said control signal input port through said first transistor differential pair; and
 - a second attenuator control signal output port, wherein said second control signal output port is coupled to said control signal input port through said second transistor differential pair.
2. The system of claim 1, wherein said RF circuit is a PIN diode attenuator circuit providing decibel per volt linear gain control by said system.
3. The system of claim 2, wherein a first control signal output at said first control signal output port is a series PIN diode bias current.
4. The system of claim 2, wherein a second control signal output at said second control signal output port is a shunt PIN diode bias current.
5. The system of claim 2, wherein a first control signal output at said first control signal output port and a second control signal output at said second control signal output cooperate to control said PIN diode attenuator circuit to provide an optimized impedance match for a return loss of said PIN diode attenuator over a dynamic attenuation range of at least 30 dB.

6. The system of claim 1, wherein said control signal input port is coupled to said first transistor differential pair at a base of one transistor of said first transistor differential pair.

7. The system of claim 6, wherein a base of another transistor of said first transistor differential pair is coupled substantially directly to a ground point.

8. The system of claim 6, further comprising:
a first current source circuit, wherein said first current source circuit is coupled to a collector of said same transistor of said first second transistor differential pair that said control signal input port is coupled to said base of.

9. The system of claim 8, wherein said first current source circuit provides a current substantially corresponding to the value $(8 K) / Z_0$, wherein K is a constant of a component of said RF circuit and Z_0 is the characteristic impedance of a system into which said RF circuit is inserted.

10. The system of claim 8, wherein said first current source circuit is programmable for use of said system with a plurality of different said RF circuit components.

11. The system of claim 8, wherein said first current source circuit is adjustable in response to temperature variations.

12. The system of claim 6, wherein a first control signal output at said first control signal output port is directly related to a collector current of another transistor of said first transistor differential pair.

13. The system of claim 1, wherein said control signal input port is coupled to said second transistor differential pair at a base of one transistor of second transistor differential pair.

14. The system of claim 13, wherein a base of another transistor of said second transistor differential pair is coupled to a ground point.

15. The system of claim 13, further comprising:
a second current source circuit, wherein said second current source circuit is coupled to an emitter of two transistors of said second transistor differential pair including said same transistor of said second transistor differential pair that said control signal input port is coupled to said base of.

16. The system of claim 15, wherein said second current source circuit provides a current substantially corresponding to the value $(2K) / (Z_0 - R_s)$, wherein K and R_s are constants of a component of said RF circuit and Z_0 is the characteristic impedance of a system into which said RF circuit is inserted.

17. The system of claim 15, wherein said second current source circuit is programmable for use of said system with a plurality of different said RF circuit components.

18. The system of claim 15, wherein said second current source circuit is adjustable in response to temperature variations.

19. The system of claim 13, wherein a second control signal output at said second control signal output port is directly related to a difference of a collector current of a transistor of said second transistor differential pair and a collector current of another transistor of said second transistor differential pair.

20. The system of claim 1, further comprising:

a first current mirror coupled to said first transistor differential pair, wherein said first control signal output port is coupled to said first transistor differential pair through said first current mirror.

21. The system of claim 1, wherein said first transistor differential pair and said second transistor differential pair each comprise a bipolar junction transistor differential pair.

22. The system of claim 1, wherein said first transistor differential pair and said second transistor differential pair each comprise a MOSFET differential pair.

23. The system of claim 1, further comprising:

a second current mirror coupled to said second transistor differential pair, wherein said second control signal output port is coupled to said second transistor differential pair through said second current mirror.

24. The system of claim 1, further comprising:

a temperature compensation circuit coupled to said control signal input port to provide temperature compensation with respect to a control signal applied thereto.

25. A system for providing linearized operation of a PIN diode attenuator, said system comprising:

a first transistor differential pair;

a second transistor differential pair;

5 a control signal input port, wherein said control signal input port accepts an attenuator control voltage applied thereto;

a first control signal output port, wherein said first control signal output port is coupled to said control signal input port through said first transistor differential pair, wherein a first control signal output at said first control signal output port is a series PIN diode bias current; and

a second attenuator control signal output port, wherein said second control signal output port is coupled to said control signal input port through said second transistor differential pair, wherein a second control signal output at said second control signal output port is a shunt PIN diode bias current.

26. The system of claim 25, wherein said control signal input port is coupled to said first and second transistor differential pairs at a base of one transistor of each of said first and second transistor differential pairs.

27. The system of claim 26, wherein a base of another transistor of each of said first and second transistor differential pairs is coupled substantially directly to a ground point.

28. The system of claim 26, wherein said first control signal output at said first control signal output port is directly related to a collector current of another transistor of said first transistor differential pair, and wherein said second control signal output at said second control signal output port is directly related to a difference of a collector current of a
5 transistor of said second transistor differential pair and a collector current of another transistor of said second transistor differential pair.

29. The system of claim 28, further comprising:

a first current source circuit, wherein said first current source circuit is coupled to a collector of said same transistor of said first second transistor differential pair that said control signal input port is coupled to said base of; and

a second current source circuit, wherein said second current source circuit is coupled to an emitter of two transistors of said second transistor differential pair including said same transistor of said second transistor differential pair that said control signal input port is coupled to said base of.

30. The system of claim 29, wherein said first current source circuit provides a current substantially corresponding to the value $(8 K) / Z_0$ and said second current source circuit provides a current substantially corresponding to the value $(2 K) / (Z_0 - R_S)$, wherein K and R_S are constants of a component of said PIN diode attenuator and Z_0 is the characteristic impedance of a system into which said PIN diode attenuator is inserted.

31. The system of claim 29, wherein said first and second current source circuits are programmable for use of said system with a plurality of different PIN diodes.

32. The system of claim 29, wherein said first and second current source circuits are adjustable in response to temperature variations.

33. A method for providing linear operation of an attenuator, said method comprising:

accepting a control signal at a linearizer input port, wherein a signal accepted at said linearizer input port is a control voltage coupled to a base of a transistor of a first transistor differential pair and a base of a transistor of a second transistor pair;

outputting a first control signal at a first linearizer output port, wherein said first control signal is a first bias current corresponding to a collector current of said first transistor differential pair; and

outputting a second control signal at a first linearizer output port, wherein said second control signal is a second bias current corresponding to a difference between collector currents of said second transistor differential pair.

34. The method of claim 33, wherein said attenuator is provided decibel per volt linear gain control by said first and second control signals.

35. The method of claim 33, wherein another collector current of said first transistor differential pair is controlled to substantially correspond to the value $(8 K) / Z_0$, wherein K is a constant of a component of said attenuator and Z_0 is the characteristic impedance of a system into which said attenuator is inserted.

36. The method of claim 33, wherein a sum of emitter currents of said second transistor differential pair is controlled to substantially correspond to the value $(2 K) / (Z_0 - R_s)$, wherein K and R_s are constants of a component of said attenuator and Z_0 is the characteristic impedance of a system into which said attenuator is inserted.

37. The method of claim 33, further comprising:
compensating said control voltage accepted at said linearizer input port for temperature.